

REMARKS

Claims 1-4 remain pending in the application. Favorable reconsideration is respectfully requested in view of the following remarks.

Claims 1, 2, and 3 again stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 4,419,724 to Branigin et al. ("Branigin") in view of U.S. Patent Number 5,649,159 to Le et al. ("Le"). This rejection is respectfully traversed.

Applicants disagree with the Office's analysis of the applied references and of their relevance to the claimed invention. It is believed that the remarks presented in Applicants' last response were not fully appreciated. Therefore, it is respectfully requested that the points made last time, and reproduced below, be given a thoughtful reconsideration.

The Office acknowledges that Branigin fails to disclose a number of Applicants' claimed features, but maintains that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Branigin by using the memory-mapped devices of Le instead of device IDs, resulting in the invention of claim 1. In particular, the Office states that Le provides the necessary teaching that a target module has an address range in the memory map including target address data and that decoding of the target address data relating to a target module is located in the initiating module. Applicants respectfully disagree for at least the following reasons.

It is respectfully asserted that one of ordinary skill in the art would not have been motivated to consider the teaching of Le in the context of the apparatus disclosed in Branigin, and would therefore not have been motivated to modify Branigin in the manner now suggested by the Office to arrive at Applicants' claimed invention. More specifically, Le discloses a microprocessor or microcontroller in which a CPU 30 (Fig. 1) includes a multi-level protection circuit to check access cycle attributes before enabling a requested transaction. The circuit (Fig. 3) includes a first and a second decoder 51, 54, each of which receives an address input 52, 55 and a control input 53, 56, the control inputs corresponding to the address inputs and representing protection attributes relevant to the addresses. Logic in the decoders generates an address match output if the address is within a respective programmable region, and an attribute match output if the corresponding control input matches a respective programmable attribute. These match outputs are input to a priority enforcing logic circuit 58 which generates an enable signal to enable access to an external device when certain logic conditions are met, these conditions permitting programmable regions to overlap or for one to be contained wholly within another.

The address decoding technique disclosed by Le is designed to maximize flexibility and, at the same time, to minimize the cost of the integrated circuit (e.g., circuit area, number of device pins and engineering effort). Although the processor 30 in the system disclosed by Le may include on-chip devices, the address decoder only operates with accesses via external bus interface 33 to off-chip devices (see column 3, line 66 to column 4, line 12).

Significantly, Le is only concerned with access to external devices initiated by the CPU. By contrast, in Applicants' claimed invention, each and every module connected to Applicant's bus architecture is able to initiate an access to any other module, subject to that module's availability. It is Applicants' contention that the person of ordinary skill in the art to which the invention pertains would not have been led to consider the teaching of Le in the context of the apparatus disclosed in Branigin and therefore the present invention. Le is concerned exclusively with a system for providing protection (e.g., preventing a write access to an external device currently engaged in a read function). The access protection technique that forms the subject of the Le patent is not concerned with the control of access to an on-chip module, as in the Applicants' invention. Moreover, it is imperative that the modules/devices connected to the bus architecture all have the same facility of initiating a transaction between modules, as compared to Le, which only has transactions initiated by the one device, the CPU.

In addition, the Le processor is designed to work with standard peripheral and memory devices. Significantly, these are "non interactive" in that they do not return the "availability data" specified in Applicant's claims. Although strictly speaking this is a feature of Branigin, the point here is that the person of ordinary skill in the art would have been even less inclined to turn to Le for information or teaching as to how to replace the device ID approach in Branigin with a memory mapped approach as required by Applicants' claims. Moreover, in Applicants' invention, the address is decoded locally by the requesting module to generate a device ID. This is all part of the distributed arbitration scheme used in a practical implementation of the invention and described in, for example, pages 20-23, which thereby saves wires and decoding logic in the arbitrator and in the target. In direct contrast, Le has to provide the full address to the peripheral devices because, apart from anything else, they are standard memory mapped devices, which is not the case in Applicants' invention.

In view of the above, it is respectfully asserted that the teaching in Le would have been such as to deter, rather than encourage, the person of ordinary skill from attempting to modify Branigin by utilizing the specific memory-mapped approach in the Le patent.

Thus, Applicants are strongly of the view that the person of ordinary skill in the art would not have been tempted or encouraged to view Le, in combination with Branigin, as a route to arriving at Applicants' claims. For at least these reasons, independent claim 1, as well as the claims 2 and 3 which depend therefrom, are believed to be patentably distinguishable over Branigin and Le, regardless of whether these documents are considered individually or in combination. Accordingly, it is respectfully requested that the rejection of these claims under 35 U.S.C. §103(a) be withdrawn.

Claim 4 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Branigan and Le as applied to Claim 1 above, and further in view of U.S. Patent Number 5,761,516 to Rostoker et al. ("Rostoker"). This rejection is respectfully traversed.

Claim 4 depends from claim 1, and is therefore patentably distinguishable over the Branigan and Le patents for at least the same reasons as set forth above. The Rostoker patent fails to make up for the deficiencies of Branigin and Le because it, too, fails to disclose or even suggest the combination of features defined by claim 1. Accordingly, claim 4 is patentably distinguishable over the Branigan, Le and Rostoker patents regardless of whether these documents are considered individually or in combination. It is therefore respectfully requested that the rejection of claim 4 under 35 U.S.C. §103(a) be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,
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